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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
09/944,073	09/04/2001	Taro Osabe	NIT-304	3764

7590 09/25/2002

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EXAMINER	
TRAN, TAN N	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/944,073	OSABE ET AL.	
	Examiner	Art Unit	
	TAN N TRAN	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 12/11/2000. It is noted, however, that applicant has not filed a certified copy of the Japan application as required by 35 U.S.C. 119(b).

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3,6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 3, line 22, "said source lines" lacks of antecedent basis.

In claim 6, line 4, "said source region and said drain region" lacks of antecedent basis.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-6,10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Takeuchi et al. (US 2002/0109539).

With regard to claims 1,2, Takeuchi et al. discloses a semiconductor device of a memory cell array of aligning plural numbers of semiconductor memory element in a matrix like manner, the element comprising: a source region 19_1; drain region 19_2; a channel region of semiconductor connecting between the source region 19_1 and the drain region 19_2; a gate electrode 16_1 made of either one of metal and semiconductor, for controlling potential of the channel region; and plural numbers of charge storage regions (14_1,14_2) formed in vicinity of the channel, wherein: a first semiconductor memory cell and a second semiconductor memory cell neighboring with each other share the source region 19_1 in common; and the second semiconductor cell shares the drain region 19_2 in common with a third semiconductor memory cell neighboring therewith. (Note lines 15-18, paragraph 006, page 1, fig.2A of Takeuchi et al.).

With regard to claims 3,4, Takeuchi et al. discloses a semiconductor device of a memory cell array of aligning plural numbers of semiconductor memory element in a matrix like manner, the element comprising: a source region 19_1; drain region 19_2; a channel region of semiconductor connecting between the source region 19_1 and the drain region 19_2; a gate electrode 16_1 made of either one of metal and semiconductor, for controlling potential of the channel region; and plural numbers of charge storage regions (14_1,14_2) formed in vicinity of the channel, wherein a layout of cell separation regions of the memory cell array is in rectangular shape, aligning them in

parallel to each other, substantially; a layout of word lines for connecting the gate electrodes of the semiconductor memory cells is in a rectangular shape aligning them in parallel to each other, substantially; the semiconductor memory cell has such structure that it shares a diffusion region of the source region 19_1 in common with only one cell neighboring therewith; source lines of at least three of the semiconductor memory cells are connected with one another through either one of diffusion layer wiring and metal wiring; and the rectangular cell separation regions of aligning in parallel to each other and the rectangular diffusion layers of aligning to each other and the rectangular cell separation region of aligning in parallel to each other and the word lines aligning in parallel to each other are perpendicular to each other in a positional relationship therebetween; the semiconductor memory cells have such structure that plural number of the source regions (19_1, 19_3) thereof are connected with each other through the diffusion layers; a layout of the diffusion layers connecting the plural numbers of the source region (19_1, 19_3) is in a rectangular shape, aligning them in parallel to each other, substantially. (Note lines 15-18, paragraph 006, and lines 1-6, paragraph 004, page 1, figs.1A,2A,3 of Takeuchi et al.).

With regard to claim 5, Takeuchi et al. discloses a channel region made of semiconductor; and plural numbers of charge storage regions (14_1,14_2) formed in vicinity of the channel region; a first gate electrode 16_1 made of either one of metal and semiconductor for controlling potential of the plural numbers the charge storage regions (14_1,14_2); and a second gate electrode 16_2 made of either one of metal and semiconductor for controlling potential of portions other than the channel region on a semiconductor surface. (Note fig.2A of Takeuchi et al.).

With regard to claim 6, Takeuchi et al. discloses a channel region made of semiconductor, connecting between source region 19_1 and drain region 19_2; plural numbers of charge storage regions (14_1,14_2) formed in vicinity of the channel region; a first gate electrode 16_1 made of either one of metal and semiconductor for controlling potential one portion of the channel region and the plural numbers the charge storage regions (14_1,14_2); and a second gate electrode 16_2 made of either one of metal and semiconductor for controlling potential of portions of the channel region other than one portion of the channel region. (Note fig.2A of Takeuchi et al.).

With regard to claim 10, Takeuchi et al. discloses the semiconductor memory cells are driven by a data line 22 and word line, wherein: drain regions (19_2,19_8) of plural numbers of semiconductor memory cells are connected to a same data line 22; second gates of the plural numbers of the semiconductor memory cells, which are connected to the same data line at the drain region thereof, are connected with each other; and first gates of the plural number of the semiconductor memory cells, which are connected to the same data line at the drain regions thereof, are connected with word lines, being different from each other. (Note fig.2A of Takeuchi et al.).

With regard to claim 11, Takeuchi et al. discloses a first semiconductor memory cell and a second semiconductor memory cell are connected, so that channel currents thereof flow in series; on one of both sides of a first gate electrode 16_1 of the first semiconductor memory cell, opposite to a second gate electrode of the second semiconductor memory cell. (Note figs.1A,2A,3 of Takeuchi et al.).

With regard to claim 12, Takeuchi et al. discloses a channel region made of semiconductor; plural numbers of charge storage regions (14_1,14_2) formed in vicinity of the channel region: a first gate electrode 16_1 made of either one of metal and semiconductor for controlling potential of the channel region and the plural numbers the charge storage regions (14_1,14_2); and a second gate electrode 16_2 made of either one of metal and semiconductor for controlling potential of portions adjacent to the channel region on a semiconductor surface; a third gate electrode 16_3 made of either one of metal and semiconductor, being formed adjacent to the channel region on the semiconductor surface, for controlling potential of a portion on an opposite side of the second gate electrode 16_2.(Note fig.2A of Takeuchi et al.).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi et al. (US 2002/0109539) in view of Fukumoto et al. (5,338,957).

With regard to claim 7, Takeuchi et al. discloses a source region 19_1; drain region 19_2; a channel region of semiconductor connecting between the source region 19_1 and the drain region 19_2; plural numbers of charge storage regions (14_1,14_2) formed in vicinity of the channel region. (Note fig.2A of Takeuchi et al.).

Takeuchi et al. does not disclose sidewall structure made of either one of semiconductor and metal, provided at both sides of the gate region; and an insulation film formed between the sidewall structures and the gate electrode.

However, Fukumoto et al. discloses sidewall structure 10 made of either one of semiconductor and metal, provided at both sides of the gate region; and an insulation film 9 formed between the sidewall structures 10 and the gate electrode 6. (Note figs. 26,41 of Fukumoto et al.).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Takeuchi et al.'s device having sidewall structure made of either one of semiconductor and metal, provided at both sides of the gate region; and an insulation film formed between the sidewall structures and the gate electrode such as taught by Fukumoto et al. in order to electrically connected to drain region 7.

With regard to claim 8, Fukumoto et al. discloses one of the sidewall structures 10 at both sides of the gate electrode 6, being near to the source region 8, is connected with the source region; and the other, being near to the drain region, is connected with the drain region 7. (Note figs. 26,41 of Fukumoto et al.).

With regard to claim 9, Fukumoto et al. discloses the sidewall structures 10 and either one of the source region 8 and the drain region 7 are connected through either one of semiconductor or metal, which is selectively piled up on the sidewall structures 10 and either one of the source region 8 and the drain region 7. (Note figs. 26,41 of Fukumoto et al.).

Conclusion

6. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (703) 305-3362. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TT

August 2002

NATHAN J. FLYNN
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